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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/778,837	02/08/2001	Norihiro Nakatsuhama	1614.1123	6812
21171 7590 03/06/2007 STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			EXAMINER BHAT, ADITYA S	
			ART UNIT 2863	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		03/06/2007	PAPER	

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

09/778,837

Applicant(s)

NAKATSUHAMA ET AL.

Examiner

Aditya S. Bhat

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 17 November 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 4-6, 8, 10 and 12 is/are allowed.
- 6) ☒ Claim(s) 1-3, 7, 9 and 11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 February 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

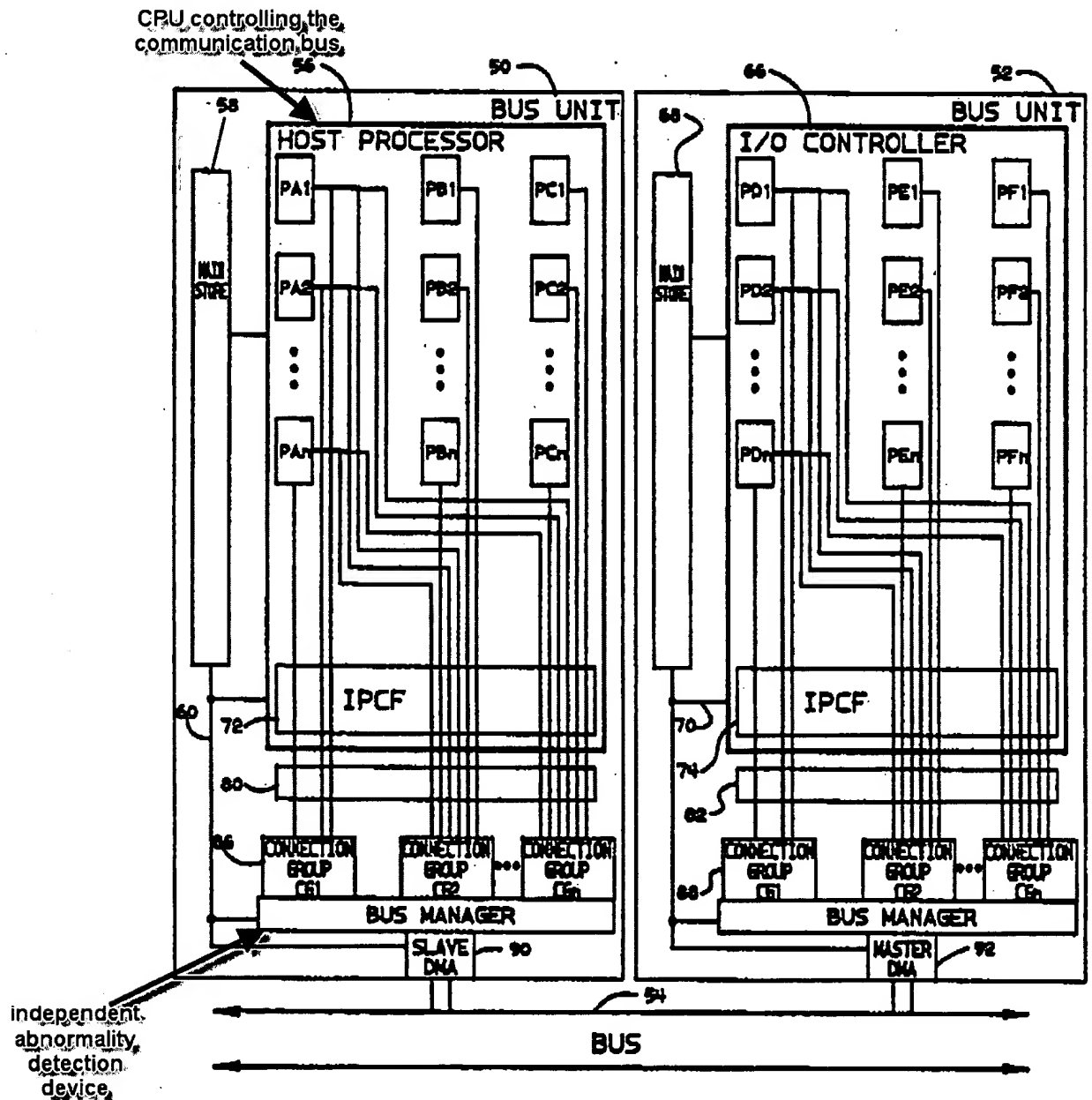
Claims 1-3, 7, 9 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Hammer (USPN 5,204,954).

Hammer (USPN 5,204,954) teaches the limitations of Claims 1 and 11 as follows an abnormality detection device for detecting an abnormality in a communication bus, the device comprising:

a timer counter (256;figure 7) configured to measure a time during which a logical output of said communication bus remains at a first logical level, which is a high level or a low level (Col. 9, lines 53-63) and

a comparator (Col. 9, line 54) configured to compare the time measured by said timer counter with a threshold value (Col. 9, line 54-55) and to output an abnormality detection signal indicating an abnormality in said communication bus when the time surpasses said threshold value, (Col. 9, line 56-57) wherein the abnormality detection device is independent of a CPU controlling the communication bus and detects the abnormality directly from the communication bus (see figure below)

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**FIG. 2**

Hammer (USPN 5,204,954) teaches the limitations of Claim 7 as follows an abnormality detection device for detecting an abnormality in a communication bus, the device comprising:

a CPU configured to control the communication bus; (56;figure 2)

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a timer counter (256;figure 7) configured to measure a time during which a logical output of said communication bus remains at a first logical level, which is a high level or a low level (Col. 9, lines 53-63) and

a comparator (Col. 9, line 54) configured to compare the time measured by said timer counter with a threshold value (Col. 9, line 54-55) and to output an abnormality detection signal indicating an abnormality in said communication bus when the time surpasses said threshold value, (Col. 9, line 56-57) wherein the abnormality detection device is independent of a CPU controlling the communication bus and detects the abnormality directly from the communication bus (see figure below)

Regarding claims 2-3, Hammer (USPN 5,204,954) teaches initializing the timer (256;figure 7) and comparator. (Col. 9, line 54) The Hammer reference teaches the use of both a comparator and a timer therefore it would be inherent for these components to be initialized at some point before use.

Regarding claim 9, Hammer (USPN 5,204,954) teaches detecting the abnormality directly from the communication by hardware. (figure 2)

### ***Allowable Subject Matter***

Claims 4 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 4,5-6,8,10 and12:

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The primary reason for the allowance of claim 4 is the inclusion of: a selector configured to store a threshold value from among said plurality of said threshold values according to a selection signal supplied thereto so as to supply said threshold value to said comparator. It is this feature found in the claim, as it is claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes this claim allowable over the prior art.

The primary reason for the allowance of claim 5 is the inclusion of: a register configured to cumulatively add the time measured by at least one of said at least two timer counters, the register being initialized at predetermined intervals. It is this feature found in the claim, as it is claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes this claim allowable over the prior art.

The primary reason for the allowance of claims 8 is the inclusion of: wherein said register supplies said cumulative time to at least one of said at least two timer counters, and said at least one of said at least two timer counters measures the time by using said cumulative time as an initial value. It is this feature found in the claim, as it is claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes this claim allowable over the prior art.

The primary reason for the allowance of claims 12 is the inclusion of: wherein said circuit supplies said cumulative time to at least one of said at least two timer counters, and said at least one of said at least two timer counters measures the time by using said cumulative time as an initial value. It is this feature found in the claim, as it is

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claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes this claim allowable over the prior art.

Claims 6 and 10 are allowed due to their dependency on claim 5.

Claims 2-8 are allowed due to their dependency on claim 1.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Imazato (USPN 6,678,858) teaches a code error monitor apparatus, Gibson(USPN 6,553,512) teaches method and apparatus for resolving CPU deadlocks, and Cathers et al. (USPN 5,511,092) teaches a data recovery technique which avoids a false convergence state.

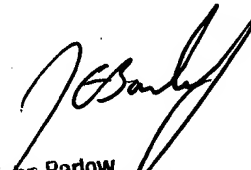
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aditya S Bhat whose telephone number is 571-272-2270. The examiner can normally be reached on M-F 9-5:30.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aditya Bhat  
February 14, 2007

  
John Barlow  
Supervisory Patent Examiner  
Technology Center 2800